IN THE SPECIFICATION

Please amend the paragraph beginning at page 2, line 15, as follows:

Furthermore, conventional transmitter designs operate so that the output power is transmitted based upon a function of many different variables. in a Code Division Multiple Access (CDMA) ~~CDMA~~ environment, for example, the power output of a mobile transmitter will typically be based upon the distance between the mobile transmitter and the base station currently in use[[d]]. In such an environment, the output power will increase, for example, if the mobile transmitter travels closer to the base station. In operation, the gain of a variable gain amplifier that is part of the transmitter, at either the intermediate frequency (IF) or radio frequency (RF) stage, will be changed to thereby lower the transmit output power. In this situation, while the output power may become too large for a period of time, that is acceptable within the overall system requirements.

Please amend the paragraph at page 3, line 3, as follows:

In other environments, however, it is required, by for instance the Federal Communication Commission (FCC), that the output power must not exceed a pre-specified level at any time. In such an environment, the above-described design cannot be used. Since in order to take into account instances in which power will exceed the pre-specified maximum, the average output power must be much lower than that maximum, which degrades system performance to an unacceptable level.

Please amend the paragraph at page 6, line 10, as follows:

Fig. 1 illustrates a block diagram of an embodiment of a power control circuit 100. As shown in Fig. 1, IF upmixer 110 upconverts signals received by the transceiver to an IF frequency as ~~frequencyas~~ is known, for example a ~~examplea~~ 1 GigaHertz IF Frequency and a 5 GigaHertz RF frequency. After the IF upmixer 110 [[130]], the IF variable gain amplifier (VGA) 130 which, in the preferred embodiment contains a 5 bit input control input and is configurable from 0 dB [[0dB]] to 15.5 dB ~~15.5dB~~ in steps of 0.5 dB ~~0.5dB~~, amplifies the IF signal. The amplified IF signal is then transmitted to an RF upmixer 178, which upconverts the IF signal to an RF signal.

Please amend the paragraph at page 7, line 9, as follows:

The outputs from each of the power detectors 182A and 182B are supplied to a comparator 188, which is strobed at appropriate intervals, described hereinafter, and the difference between the transmitted signal and the reference signal obtained from the comparator 188 is input to power control circuit 190. As described further hereinafter with respect to Fig. 2, the power control circuit 190 is used to achieve and maintain a steady state operation, such that on a packet-to-packet basis the gain settings of the variable gain amplifier 130 desirably ~~130desirably~~ results in a substantially constant output power. While the variable gain amplifier 130 is described hereinafter as a single gain stage containing numerous gain cells, it is noted that a number of variable gain amplifiers, in both IF and RF transmitter portions, could instead be used, with the composite gain then being determined and used by the power control circuit 190 as described herein.

Please amend the paragraph beginning at page 8, line 21, as follows:

If, however, in step 204 a normal operation mode occurs, then gainSelect flag will be set to "0", and the gain used will set the variable gain amplifier 130 to a normal mode operation initial gain value. In this state, the first few data symbols, such as the first eight, that are transmitted will preferably have known, deterministic initial values, thus allowing the power control circuit to achieve a steady state condition more accurately. In a preferred embodiment, gain control is only performed on some initial number of the first few data symbols, such as 5, so that the remaining symbols having deterministic values can be used for automatic gain control (AGC) in the receiver which is receiving the transmitted signal. Further, in the preferred embodiment, each symbol is 0.8 µs ~~0.8□s~~ long, such that if gain changes occur during the first 5 symbols this provides 4 µs [[4□s]] for obtaining the appropriate gain, and each packet is about 1 ms [[1ms]] in duration.

Please amend the paragraph at page 9, line 9, as follows:

Once the gain setting for the VGA 130 is obtained and the power amplifier 180 becomes turned on, then the normal mode operation initial gain value will be used to initially operate the variable gain amplifier 130 ~~amplifier130~~ for the remainder of the packet transmission. An initial wait step 206 then follows, and allows the system to settle at this initial gain value. The initial wait time can be predetermined, but will typically be longer than the wait time that is used between gain steps as described hereinafter.

Please amend the paragraph beginning at page 9, line 19, as follows:

In the preferred embodiment, the gain may be increased in 0.5 dB ~~0.5dB~~ increments, although in early steps if the gain is lower than the desired gain by some predetermined threshold, steps as large as 2.0 dB ~~2.0dB~~ can be initially used. No matter what gain steps are used, however, an important aspect of the present invention is that an individual gain step will not cause the overall power of the transmitted signal to exceed a predetermined maximum value, which value will typically correspond to FCC regulations, as noted above. Also during step 208, the next wait interval is set, which again can be up to 2 µs in 62.5 ns ~~2us in 62.5ns~~ steps in the preferred embodiment.

Please amend the paragraph beginning at page 11, line 15, as follows:

Fig. 3 shows the inductively-loaded folded-cascode level-shift stage between the upmixer 110 and the variable gain amplifier 130 in more detail. The IF upmixer 110, which will either take the baseband signal to an IF level as described in the preferred embodiment, as well as the RF upmixer 178, which will take the IF signal to an RF level, can be formed using conventional techniques. The present invention provides, however, an inductively tuned level-shift stage at the output of the IF mixer 110. The differential output signal, shown as DP (positive) 115 and DN (negative) 113, that is output from the mixer 112, is transmitted through an inductively loaded folded cascode circuit. P-type metal-oxide-semiconductor (PMOS) ~~PMOS~~ transistors 118 and 120, with each gate thereof biased at a DC bias that will result in a fixed, predetermined DC drain current flowing through the PMOS transistors 122 and 124, [[,]] complete the level-shift circuit at the output of mixer 110. The purpose of the level-shift block is to convert the

~~VDD~~ Voltage Drain-Drain (VDD)-referenced driver output of the upmixer circuit 110 to a ground-referenced signal suitable for driving an n-type metal-oxide-semiconductor (NMOS) ~~NMOS~~ current mirror, as well as to convert the differential outputs of the upmixer circuit 110 into low-impedance (current-mode) nodes, thereby making the upmixer circuit less sensitive to the quality factor (Q) of the tuned output load. Put another way, the level-shift block with the PMOS common gate stage operates as a folded-cascode stage with unity current gain, redirecting AC current from the upmixer circuit 110 to ground.

Please amend the paragraph at page 12, line 15 as follows:

The input current load block 132 of Fig. 4 will first be described in more detail, and contains NMOS transistors 134, 163, 138 and 140, with the gates of NMOS transistors 134 and 136 being biased by the first DC voltage and which together function as cascode transistors for the current mirror transistor 138 and 140. [[.]] The gate of each of transistors 138 and 140, and the drain of each of transistors 134 and 135, respectively receive the INP and INN input signals, which are output from the input current load block as signals gn [[GN]] and gp, [[GP,]] as shown.

Please amend the paragraph beginning at page 12, line 22, as follows:

The switch network 142 of Fig. 4 will next be described in more detail and contains PMOS transistors 144 and 148, and NMOS transistors 146, and 150. Transistors 144 and 146 operate as a pair and are used to switch the cascode voltage at the gates of transistors 134 and 136 to the outer pair of transistors 162 and 170 of the gain cell block 160, as described further hereinafter, whereas transistors 148 and 150 operate as a pair and are used to switch the cascode voltage at the gates of transistors 134 and 136 to the inner pair of transistors 164 and 168 of the gain cell 160. Each of transistors 144 and 146 are switched based upon the pos_b ~~POS_B~~ input signal, whereas each of transistors 148 and 150 are switched based upon the neg_b ~~NEG_B~~ input signal. In operation, either one of pos_b ~~POS_B~~ or neg_b ~~NEG_B~~ may be on at the same time, but both will not be on at the same time. It is also noted that PMOS transistors 144 and 148 have their bulk node tied to their source nodes providing lower on-resistance, which improves their switch characteristics, and that the size of the transistors 144, 146, 148 and 150 is fixed, and not related to the size of any other deices, unlike the transistors in the input current load block 132 and gain cell 160, which are chosen to mirror each other, as described further herein.

Please amend the paragraph at page 13, line 14, as follows:

Each gain cell 160, such as the gain cell 160-1 of Fig. 4, is essentially an NMOS current mirror, formed of transistors 162-172. Before further describing a gain cell 160, it is noted that the current outputs from the gain cell 160 mirror the current inputs inp [[INP]] and inn [[INN]] presented to the input current load block 132. The sizing of the transistors 162, 164, 168 and 170 thus mirror the size of the transistors 134-140 from the input current load block 132.

Please amend the paragraph beginning at page 13, line 19, as follows:

With transistor 166 having its gate controlled by the gp [[GP]] signal, and transistor 172 having its gate controlled by the gn [[GN]] signal, and possibly either transistors 162 and 170, or 164 and 168 turned on, depending upon the state of the pos_b ~~POS_B~~ and neg_b ~~NEG_B~~ signals, each gain cell is provided with two gain settings: a positive polarity setting and a negative polarity setting. In the positive gain setting, current from transistors 166 and 172 flows through transistors 162 and 170, respectively, in a conventional current mirror configuration. In the negative gain setting, the drain outputs of the current mirrors are reversed, and current from transistors 166 and 172 flows through transistors 164 and 168, respectively, resulting in a current mirror cell with the same AC gain, but opposite polarity.

Regarding the paragraph at page 14, line 5, Figure 4 has been modified to show "OUTN" and "OUTP." Please amend the paragraph at page 14, line 5 as follows:

In operation, as noted, multiple ones of the gain cells 160 in the variable gain amplifier 130 will be connected in parallel such that two signals, ~~GN~~ gn and gp ~~GP~~, drive the common gn ~~GN~~ and gp ~~GP~~ input of all of the gain cells, and two outputs, OUTN and OUTP, will be driven by the common OUTN and OUTP outputs of all of the gain cells. This type of parallel connection of multiple gain cells allows for small incremental gain steps. In operation, there should always be more "positively-connected" gain cells than "negatively-connected" gain cells, resulting in an overall positive configuration.

Please amend the paragraph at page 14, line 12, as follows:

Within the variable gain amplifier 130, a single one of the gain cells 160 ~~cell 160,' which is constructed the same as the gain cell 160 previously described is included. In operation, the gain cell 160'~~ (i.e. "fine adjust cell") can be both "positively-connected" and "negatively-connected," thereby allowing it to be placed in a neutral gain configuration and allowing for fine adjustments to be made by simply turning this ~~gain~~ fine adjust cell on or off, and effectively allowing the gain increment to be half of what it would be without this ~~gain~~ fine adjust cell ~~160'~~ 160. Thus, for example, if gains are stepped through at 0.5 dB, 1.0 dB, 1.5 dB, 2.0 dB, 2.5 dB, and 3.0 dB ~~0.5dB, 1.0dB, 1.5dB, 2.0dB, 2.5dB, and 3.0dB~~, the fine adjust cell will change state several times. It should also be noted that each of the various pos_b ~~POS_B~~ and neg_b ~~NEG_B~~ signals is controlled by the power control circuit, which, as described, operates digitally. Accordingly, it will be appreciated that the relative size of each gain step can be precisely controlled, since each gain step may be a combination of both positively connected gain cells and negatively connected gain cells.